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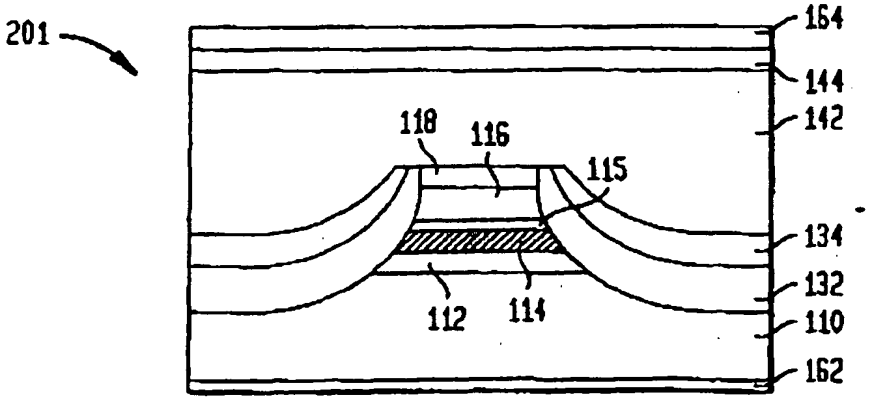
(54) Dopant diffusion blocking for optoelectronic devices using InAlAs or InGaAlAs

(57) A method for decreasing the diffusion of dopant atoms in the active region, as well as the interdiffusion of different types of dopant atoms among adjacent doped regions, of optoelectronic devices is disclosed. The method of the present invention employs a plurality of InAlAs and/or InGaAlAs layers to avoid the direct contact between the dopant atoms and the active region, and between the dopant atoms in adjacent blocking structures of optoelectronic devices. A semi-insulating buried ridge structure, as well as a ridge structure, in which the interdiffusion of different types of dopant atoms is suppressed are also disclosed.

FIG. 13



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Description

Field of the Invention

[0001] The present invention relates to a method for fabricating optoelectronic devices, such as lasers, modulators, optical amplifiers, and detectors, and in particular to a method and device for reducing the diffusion and/or interdiffusion of dopant atoms among differently doped regions of such optoelectronic devices.

Background of the Invention

[0002] Blocking layers are increasingly important for optoelectronic devices. For example, in a buried heterostructure of a semiconductor laser diode, blocking layers confer superior characteristics, such as low oscillatory threshold value and stable oscillation transverse mode, as well as high quantum efficiency and high characteristic temperature. This is because, in the buried heterostructure laser diodes, a current blocking layer can be formed on both sides of an active layer formed between two clad layers having a large energy gap and a small refractive index. This way, current leakage during operation is substantially reduced, if not prevented.

[0003] A conventional method for the fabrication of semiconductor laser diodes having a semi-insulating buried ridge is exemplified in Figures 1-7 and described below.

[0004] Referring to Figure 1, the processing steps for fabricating a laser diode with a buried ridge begin with the formation of a multi layered structure 100 on an n-InP substrate 10. The multi layered structure 100 is formed of a first n-InP cladding layer 12, an active layer 14, a second p-InP cladding layer 16, and a layer 18 of a quaternary material (Q). Layers 12, 14, 16 and 18 are sequentially formed and successively epitaxially grown to complete a first crystal growth. The active layer 14 could be, for example, a multiple quantum well (MQW) structure formed of undoped InGaAs/InGaAsP pairs and formed by a Metal Organic Chemical Vapor Deposition (MOCVD) or Metal Organic Vapor Phase Epitaxy (MOVPE). Also, the second cladding layer 16 may be doped with a p-type dopant, the most common one being zinc (Zn).

[0005] Next, as shown in Figure 2, a SiO_2 or Si_3N_4 mask 20 is formed into a stripe on the upper surface of layer 18. Subsequently, the multi layered structure 100 is selectively etched down to the n-InP substrate 10 to produce a mesa stripe 50, as illustrated in Figure 3. The mesa stripe 50, which has the mask 20 on top, is then introduced into a growth system, such as a liquid phase pitaxial, a MOCVD, a molecular beam epitaxy (MBE), or vapor phase epitaxy (VPE) growth system, so that an InP current blocking lay r 32 and an n-InP curr nt blocking lay r 34 are subsequently formed, as shown in Figure 4. The current blocking layers 32 and 34 surround the mesa stripe 50 and form a second crystal growth.

[0006] The first current blocking layer 32 may be doped with impurity ions, such as iron (F), ruthenium (Ru) or titanium (Ti), to form a semi-insulating (si) InP (Fe) blocking layer 32. The addition of Fe-impurity ions increases the resistivity of the first current blocking layer 32 and reduces the leakage current that typically occurs at the interface between the substrate 10 and the first current blocking layer 32. Similarly, the second current blocking layer 34 may be doped with impurity ions, such as silicon (Si), sulfur (S) or tin (Sn), to form an n-typ InP-doped blocking layer 34.

[0007] Referring now to Figure 5, after removal of th mask 20, a third crystal growth is performed on the upper surfaces of the second current blocking layer 34 and the Q layer 18. Thus, a p-InP cladding layer 42 (also called a burying layer) and a p-InGaAsP or a p-InGaAs ohmic contact layer 44 are further grown to form a buried heterostructure. The cladding layer 42 may be also doped with p-type impurity ions, such as zinc (Zn), magnesium (Mg), or beryllium (Be), to form a p-type InP-doped cladding layer 42. Since Zn is the most commonly used p-type dopant, the cladding layer 42 will be r - ferred to as layer InP(Zn)-doped.

[0008] The method of fabricating the above structure poses three major drawbacks, all of them relating to the diffusion and interdiffusion of dopant atoms, particularly those of zinc, since zinc is the most common and widely used p-type dopant in the optoelectronic industry.

[0009] First, zinc diffusion occurs into the active region of the semi-insulating buried ridge. Figure 5 shows the diffusion of zinc in the direction of arrow A, from the doped p-InP(Zn) second cladding layer 16 into the active layer 14, because of the direct contact between the two layers. The high diffusivity of zinc leads to an undesirable shift in the emitting wavelength, up to tenths of microns. The reshaping of the overall zinc distribution profile further impacts the electrical characteristics of the optoelectronic device. The excess of zinc in the active region 14 of the device structure also results in th degradation of various device characteristics, such as the extinction ratio and the junction capacitance of the electro-absorption modulator structures.

[0010] Second, iron-zinc (Fe-Zn) interdiffusion occurs at the interface between the doped p-InP(Zn) second cladding layer 16 and the semi-insulating InP(Pe) first current blocking layer 32. Figure 5 shows the diffusion of zinc in the direction of arrow B_1, from the p-InP(Zn) second cladding layer 16 into the InP(Fe) first current blocking layer 32. Similarly, arrow B_2 of Figure 5 illustrates the diffusion of iron from the InP(Fe) first current blocking layer 32 into the p-InP(Zn) second cladding layer 16.

[0011] Third, iron-zinc (Fe-Zn) interdiffusion occurs in the blocking structures of the laser devices, more pr - cis ly at the interface betw en the semi-insulating InP (F) first current blocking lay r 32 and the p-InP(Zn) cladding layer 42. The problem arises because the Fe-doped InP current blocking layer 32, which was initially

covered by the mask 20, comes into contact with the Zn-doped InP cladding layer 42 after the removal of the mask 20. The contact regions are exemplified in Figures 5 as regions D, situated on lateral sides of the mesa stripe 50. The interdiffusion of Fe and Zn atoms at the regions D can significantly increase the leakage current and degrade the device, leading to a poor manufacturing yield. In addition, if the active layer 14 has a multiple quantum well (MQW) structure, the Zn impurities in the Zn-doped InP cladding layer 42 can enter the active layer 14 to form mixed crystals therein and practically reduce the quantum effect to zero.

[0012] In an effort to suppress the diffusion and interdiffusion of Zn dopant atoms, different techniques have been introduced in the IC fabrication, For example, one technique of the prior art, shown in Figure 6, considered the incorporation of a zinc doping set-back into the device structure, such as an undoped InP layer 52. The undoped InP layer 52 is grown after the growth of the active layer 14, but before the growth of the p-InP second cladding layer 16, to prevent therefore the direct contact between zinc and the active region. In lieu of the undoped InP layer 52, a silicon doped n-InP(Si) layer may bc uscd also as a dopant set-back.

[0013] Although the above technique has good results in preventing the Zn diffusion, its processing steps require extremely sensitive parameters, such as doping level and thickness, of the zinc-doped cladding and contact layers. Also, growth conditions, such as growth rate and temperature, must be very narrowly tailored so that the set-back is optimized for each device structure and for each reactor. Further, this method does not allow control over the shape of the final zinc distribution. Finally, when a silicon doped n-InP(Si) layer is alternatively used as a dopant set-back, the incorporated silicon, which is an n-type dopant, forms an additional and undesirable p-n junction on the p-side of the device.

[0014] Another technique of the prior art that tried to minimize the zinc-iron interdiffusion is exemplified in Figure 7. This technique contemplates the insertion of an intrinsic or undoped InP layer 70 between the Fe-doped InP current blocking layer 32 and the Zn-doped InP cladding layer 42, to prevent the contact between the InP(Fe) layer and InP(Zn) layer and to eliminate the iron-zinc interdiffusion and the consequent leakage current. This technique, however, has a major drawback in that it affects the p-n junction between the n-InP second current blocking layer 34 and the p-InP burying layer 42. Specifically, the addition of an intrinsic InP layer modifies the p-n junction that should be in the active region of a laser device; and creates instead a p-i-n junction that alters the device characteristics altogether. Further, this method is insufficient to completely prevent the iron-zinc interdiffusion in areas close to the active region of the device.

[0015] Accordingly, a method for forming a mesa strip for optoelectronic d vices, which is inexpensiv to implement and capable of decreasing the leakage current and the interdiffusion of dopant stoms is ne ded. There is also a need for an optoelectronic semiconductor device having good operating characteristics with reduced impurity atoms interdiffusion, reduced leakage current, and improved accuracy and operation reliability.

Summary of the Invention

[0016] The present invention provides a method for reducing the diffusion and/or interdiffusion of dopant atoms between differently doped regions of semi-insulating buried ridge structures of forward biased devices, such as lasers and optical amplifiers, and of reverse biased devices, such as electroabsorption modulators and detectors.

[0017] In a first embodiment of the present invention, either an InAlAs (indium aluminum arsenide) or an InGaAlAs (indium gallium aluminum arsenide) layer is grown on top of the active region, and before the zinc-doped cladding layer and the subsequent contact layer are grown. The blocking of zinc diffusion into the activ layer by the insertion of a thin InAlAs or InGaAlAs layer allows a precise placement of the p-i junction, at less than 100 Angstroms, as well as minimal doping into th active region.

[0018] In a second embodiment of the present invention, an InAlAs or an InGaAlAs layer is first selectiv ly grown on top of the active region and around the mesa structure, and only then are conventional InP and n-InP current blocking layers, which form a second crystal growth around the mesa, grown over the InAlAs or InGaAlAs layer. This way, the lateral interdiffusion between Fe atoms, from the InP(Fe) current blocking layer, and the Zn atoms, from the p-InP(Zn) second cladding layer situated on top of the active region, is suppressed since no contact between the two doped regions exists.

[0019] In yet a third embodiment of the invention, a plurality of InAlAs and/or InGaAlAs layers are grown on top of the active region and around the mesa structure, as well as in lieu of the conventional second current blocking layer of the second crystal growth.

[0020] A fourth embodiment of the present invention is structurally similar to the third embodiment. However, in the fourth embodiment, the InP(Fe) current blocking layer is grown between two adjacent InAlAs and/or InGaAlAs layers, so that the InP(Fe) layer has minimal contact with the mask situated on top of the mesa strip .

[0021] According to fifth and sixth embodiments of the present invention, a plurality of InAlAs and/or InGaAlAs layers are grown on top of the active region and around the mesa structure, as well as in between the blocking layers forming the second crystal growth. In the fifth embodiment, an InAlAs and/or InGaAlAs layer is grown after the two current blocking layers have been formed and as part of the second crystal growth. Conversely, in the sixth mbodiment, an InAlAs and/or InGaAlAs layer is grown as part of the third crystal growth and before the top cladding layer is formed. In any case, these mul-

tiple InAlAs and/or InGaAlAs layers suppress the interdiffusion between Fe atoms, from the InP(Fe) current blocking layer, and the Zn atoms, from the p-InP(Zn) cladding layer of the third crystal growth. Multiple InAlAs and/or InGaAlAs layers may be incorporated in the blocking and/or cladding structures to confer optimized performance to the optoelectronic devices.

[0022] The above and other advantages of the present invention will be better understood from the following detailed description of the preferred embodiments, which is provided in connection with the accompanying drawings.

Brief Description of the Drawings

[0023] Figure 1 illustrates a cross-sectional view of a buried heterostructure laser diode at an intermediate stage of processing in accordance with a method of the prior art.

[0024] Figure 2 is a cross-sectional view of the buried heterostructure laser diode of Figure 1, in accordance with a method of the prior art and at a stage of processing subsequent to that shown in Figure 1.

[0025] Figure 3 is a cross-sectional view of the buried heterostructure laser diode of Figure 1 at a stage of processing subsequent to that shown in Figure 2.

[0026] Figure 4 is a cross-sectional view of the buried heterostructure laser diode of Figure 1 at a stage of processing subsequent to that shown in Figure 3.

[0027] Figure 5 is a cross-sectional view of the buried heterostructure laser diode of Figure 1 at a stage of processing subsequent to that shown in Figure 4.

[0028] Figure 6 is a cross-sectional view of a modified buried heterostructure laser diode of Figure 1 and depicting an undoped InP layer grown on the active region of the laser diode.

[0029] Figure 7 is a cross-sectional view of the buried heterostructure laser diode of Figure 1 at a stage of processing subsequent to that shown in Figure 5, and depicting an intrinsic InP layer.

[0030] Figure 8 illustrates a cross-sectional view of a buried heterostructure laser diode at an intermediate stage of processing and in accordance with a first embodiment of the present invention.

[0031] Figure 9 is a cross-sectional view of the buried heterostructure laser diode of Figure 8 at a stage of processing subsequent to that shown in Figure 8.

[0032] Figure 10 is a cross-sectional view of the buried heterostructure laser diode of Figure 8 at a stage of processing subsequent to that shown in Figure 9.

[0033] Figure 11 is a cross-sectional view of the buried heterostructure laser diode of Figure 8 at a stage of processing subsequent to that shown in Figure 10.

[0034] Figure 12 is a cross-sectional view of the buried het rostructur las r diode of Figure 8 at a stag of processing subsequent to that shown in Figure 11.

[0035] Figure 13 is a cross-sectional view of the buried heterostructure laser diode of Figure 8 at a stage of processing subsequent to that shown in Figure 12.

[0036] Figure 14 is a cross-sectional view of a buried heterostructure laser diode at an intermediate stage of processing and in accordance with a second embodiment of the present invention.

[0037] Figure 15 is a cross-sectional view of the buried heterostructure laser diode of Figure 14 at a stage of processing subsequent to that shown in Figure 14.

[0038] Figure 16 is a cross-sectional view of the buried heterostructure laser diode of Figure 14 at a stage of processing subsequent to that shown in Figure 15.

[0039] Figure 17 is a cross-sectional view of the buried heterostructure laser diode of Figure 14 at a stage of processing subsequent to that shown in Figure 16.

[0040] Figure 18 is a cross-sectional view of the buried heterostructure laser diode of Figure 17 but which includes an InAlAs or InGaAlAs layer on top of the activ region of the heterostructure laser diode.

[0041] Figure 19 is a cross-sectional view of a buried heterostructure laser diode at an intermediate stage of processing and in accordance with a third embodiment of the present invention.

[0042] Figure 20 is a cross-sectional view of a buried heterostructure laser diode at an intermediate stage of processing and in accordance with a fourth embodiment of the present invention.

[0043] Figure 21 is a cross-sectional view of the buried heterostructure laser diode of Figure 20 at a stage of processing subsequent to that shown in Figure 20.

[0044] Figure 22 is a cross-sectional view of a buried heterostructure laser diode at an intermediate stage of processing and in accordance with a fifth embodiment of the present invention.

[0045] Figure 23 is a cross-sectional view of the buried heterostructure laser diode of Figure 22 at a stage of processing subsequent to that shown in Figure 22.

[0046] Figure 24 is a cross-sectional view of a buried heterostructure laser diode at an intermediate stage of processing and in accordance with a sixth embodiment of the present invention.

[0047] Figure 25 is a cross-sectional view of a further embodiment of the present invention depicting a ridg structure for an optelectronic device at an intermediate stage in the processing.

Detailed Description of the Preferred Embodiments

[0048] In the following detailed description, reference is made to various specific embodiments in which the invention may be practiced. These embodiments are described with sufficient detail to enable those skilled in the art to practice the invention, and it is to be und r-stood that other embodiments may be employed, and that structural and electrical changes may be made without departing from the invention. Accordingly, the following d tailed d scription is not to be taken in a limiting sense and the scope of the present invention is defined by the appended claims.

[0049] The present invention provides a method for decreasing the diffusion of dopant atoms in the active region, as well as the interdiffusion of different types of dopant atoms among adjacent doped regions of semi-insulating buried ridge structures of laser devices or optical amplifiers, and of ridge structures of electroabsorption modulators or detectors. The method of the present invention employs a plurality of InAlAs and/or InGaAlAs layers to avoid the direct contact between the dopant atoms and the active region, and between the dopant atoms in adjacent blocking structures of optoelectronic devices.

[0050] The term "p-type dopant" used in the following description may include any p-type impurity ions, such as zinc (Zn), magnesium (Mg), or beryllium (Be), among others. Since Zn is the most commonly used p-type dopant, reference to the p-type dopant will be made in this application as to Zn dopant. Although the present invention will be described and demonstrated above with respect to Zn dopant, it is anticipated that the plurality of InAlAs and/or InGaAlAs layers of the present invention will serve to block other p-type dopants as well.

[0051] Similarly, the term "n-type dopant" used in the following description may include any n-type impurity ions, such as silicon (Si), sulfur (S), or tin (Sn), among others. Although reference to the n-type dopant will be made in this application as to Si dopant, and although the present invention will be described with respect to Si dopant, it is anticipated that the plurality of InAlAs and/or InGaAlAs layers of the present invention will serve to block other n-type dopants as well.

[0052] The term "semi-insulating-type impurity" used in the following description may include any impurity ions, such as iron (Fe), ruthenium (Ru) or titanium (Ti), that form semi-insulating blocking layers. Since Fe is the most commonly used semi-insulating type impurity, reference to the semi-insulating-type dopant will be made in this application as to Fe dopant. Also, although the present invention will be described and demonstrated above with respect to Fe, it is anticipated that the plurality of InAlAs and/or InGaAlAs layers of the present invention will serve to block other semiinsulating-type dopants as well. Accordingly, the following detailed description must not be taken in a limiting sense, the scope of the present invention being defined by the appended claims.

[0053] Referring now to the drawings, where like elements are designated by like reference numerals, Figures 8-13 illustrate the fabrication method of the first embodiment of a buried semi-insulating ridge heterostructure 201 (Figure 13) of the present invention, in which Zn diffusion into the active region of the optoelectronic device is suppressed.

[0054] First, as shown in Figure 8, preferably on an n-InP substrate 110 having a <100> plane as a main plane, a first cladding lay r 112 of n-InP and an active layer 114 having a quantum well structure of InGaAsP are preferably successively epitaxially grown. It must be noted that, although the Metal Organic Vapor Phase Epitaxy (MOVPE) method is preferred, a Liquid Phase Epitaxy (LPE) method, a Vapor Phase Epitaxy (VPE) method, or a Molecular Beam Epitaxy (MBE) could also be used as an alternative. As known in the art, the active layer 114 should be capable of absorbing, emitting, amplifying, or modulating light, depending on the particular type of optoelectronic device. Also, although the present invention refers to an exemplary n-type substrate on which operative layers form an n-p junction around an active area, it is to be understood that the present invention also contemplates a p-type substrate on which a corresponding p-n junction is formed around an active area.

[0055] Further, although the embodiments of the present invention will be described below with reference to an InAlAs layer as blocking the diffusion and/or interdiffusion of different types of dopant impurities, it must be understood that same processing conditions and proceedings are applicable for an InGaAlAs layer used as a diffusion blocking layer. Thus, the present invention is not limited to the use of InAlAs as a dopant diffusion blocking layer, and the invention has equal applicability to the use of InGaAlAs as a dopant diffusion blocking layer, or a combination of InAlAs and InGaAlAs lay rs.

[0056] As next illustrated in Figure 9, an InAlAs lay r 115 is formed on top of the active layer 114. The InAlAs layer 115 may be, for example, epitaxially grown up to a thickness of between approximately 300 Angstroms to approximately 800 Angstroms, by either the MOVPE or the LPE method. Although the embodiments of the present invention will be described with reference to the InAlAs and/or InGaAlAs layer 115 being formed on top of the active region 114, it must be understood that the active region may be also bounded on at least one side by the dopant blocking layer. The term "bounded" in the context of this application means that the dopant blocking layer is in contact or spaced apart from the active region through another region or layer. In any case, the InAlAs layer 115 acts as a zinc diffusion barrier layer, blocking the diffusion of Zn atoms from the subsequently grown upper layers into the active layer 114.

[0057] The incorporation of a thin layer of InAlAs offers an additional advantage. That is, the InAlAs layer does not introduce excess potential barriers for majority carriers or holes, since the InAlAs layer forms type II heterojunctions with the adjacent layers, the active layer (for example, the active layer 114 of Figure 10) and the cladding layer (for example, the cladding layer 116 of Figure 10). The InAlAs layer has a band gap (E=1,44eV) that is higher than the band gap of the active region (E=0.8eV) and than the band gap of the adjacent cladding layer (for example, E=1,35eV for the InP cladding layer 116). Because of these differences, no body of carri rs is created betw en the cladding layer and the active region because of the lineup of th band gaps.

[0058] Next, after the formation of the InAlAs layer 115, the processing steps for the formation of a semi-

insulating buried ridge of a laser diode proceed according to the steps described with reference to Figures 1-5, and in accordance with the prior art. As such, a second cladding layer 116 preferably of p-InP doped with Zn and a Q layer 118 are preferably epitaxially grown, as illustrated in Figure 10. Using a silicon oxide or silicon nitride mask 200 (Figure 10), the multi layered structure of Figure 10 is etched down to the n-InP substrate 110 to form a narrow striped-shaped ridge structure, or a mesa stripe, 150 (Figure 11) on the substrate 110. The etching may be carried out by using, for example, a conventional Br-methanol solution or a solution comprising a mixture of oxygenated water and hydrochloric acid.

[0059] The striped-shaped ridge structure 150 of Figure 11, which is similar to that represented in Figure 3, comprises portions of the first cladding layer 112 of n-InP, of the active layer 114, of the InAlAs zinc blocking layer 115, of the second cladding layer 116 of p-InP(Zn), and of the Q layer 118. As illustrated in Figure 11, the striped-shaped ridge structure 150 resides on an upper surface of the n-InP substrate 110.

[0060] Thereafter, striped-shaped ridge structure 150, which has on top the mask 200, is introduced into a liquid phase epitaxial growth system or a MOCVD growth system to preferably form a first InP current blocking layer 132 and an n-InP current blocking layer 134, as shown in Figure 12. Preferably, the current blocking layers 132 and 134 are grown selectively by Metal Organic Vapor Phase Epitaxy (MOVPE) around the striped-shaped ridge structure 150. The current blocking layer 132 is preferably doped with a semi-insulating type dopant, such as iron (Fe), ruthenium (Rn), or titanium (Ti), in the range of $1x10^{18}cm^{-3}$ to $3x10^{18}cm^{-3}$, to achieve the semi-insulating (si) InP-doped current blocking layer, in our case the first semi-insulating current blocking layer InP(Fe) 132 (Figure 12). Similarly, the second current blocking layer 134 may be doped with impurity ions such as silicon (Si), sulfur (S), or tin (Sn) to form an n-type InP-doped blocking layer 134.

[0061] Referring now to Figure 13, after removal of the mask 200 and the optional removal of the Q layer 118, a third crystal growth is performed on the upper surfaces of the second current blocking layer 134 and the Q layer 118. Although the embodiments of the present invention are described as having the Q layer 118 incorporated into the mesa structure, it must be understood that the present invention also contemplates optoelectronic devices that do not include a Q layer, such as Q layer 118 (Figures 10-24). Further, although the embodiments of the present invention are described as having a first and a second current blocking layers, such as current blocking layers 132 and 134 (Figures 12-13; Figures 16-18; Figures 22-24), it must be understood that the present invention also contemplates optoelectronic devices with more than two current blocking layers as part of the second crystal growth, for xample four current blocking layers with alternate doping conductivity.

[0062] As part of the third crystal growth, preferably a p-InP cladding layer 142 (Figur 13) and a p-InGaAsP or a p-InGaAs ohmic contact layer 144 (Figur 13) are further grown to form a buried heterostructure. The cladding layer 142 is preferably liquid-phase epitaxially grown or MOCVD grown to a thickness of 1.5 to 3 microns, preferably 2.5 microns, and doped with a p-type impurity atom, such as zinc (Zn), magnesium (Mg) or beryllium (Be). For example, doping can be conducted with diethyl zinc (DEZ), with H2 as carrier gas and at varying temperatures, from approximately -15°C to 40°C. Similarly, the ohmic contact layer 144 may be, for example, a Zn-doped InGaAs preferably epitaxially grown layer, to a thickness of approximately 3000 Angstroms.

[0063] An n-type electrode 162 (Figure 13) is formed on the lower surface of the substrate 110 and a p-type electrode 164 (Figure 13) is formed on the upper surface of the ohmic contact layer 144, to supply a voltage to the buried semi-insulating ridge heterostructure 201 which has an InAlAs 115 layer for blocking zinc diffusion into the active region 114 of the heterostructure.

[0064] In a second embodiment of the present inv n-tion (Figures 14-18), an InAlAs layer is selectively grown before the formation of the current blocking layers, which constitute the second crystal growth. To illustrat the second embodiment, reference is now made to Figure 14, which illustrates a striped-shaped ridge structure (mesa stripe) 151, which is similar to the striped-shaped ridge structure 150 of Figure 11 but without the InAlAs layer 115. Thus, the striped-shaped ridge 151 comprises portions of a first n-InP cladding layer 112, of the active layer 114, of the second p-InP(Zn) cladding layer 116, and of a Q layer 118. As illustrated in Figure 14, the striped-shaped ridge 151 resides on an upper surfac of the n-InP substrate 110.

[0065] Referring now to Figure 15, the mesa stripe 151 of Figure 14 is then introduced into a liquid phase epitaxial growth system or a MOCVD growth system to form an InAlAs layer 131. Preferably, the InAlAs layer 131 is grown selectively by Metal Organic Vapor Phase Epitaxy (MOVPE) around the striped-shaped ridge structure 151 and parts of the n-InP substrate 110. Th InAlAs layer 131 may be epitaxially grown up to a thickness of between approximately 300 Angstroms to approximately 3000 Angstroms, sufficient to allow InAlAs layer 131 to suppress the zinc-iron lateral interdiffusion between the subsequently grown current blocking layers.

[0066] The InP first current blocking layer 132 (Figure 16) is subsequently epitaxially grown around the striped-shaped ridge structure 151 and over the InAlAs layer 131. As explained above with reference to the first embodiment, the first current blocking layer 132 (Figures 12-13; Figure 16) is doped with a semi-insulating type dopant, such as iron (F), in the range of $1x10^{18}cm^{-3}$ to $3x10^{18}cm^{-3}$, to form the semi-insulating InP(Fe) first current blocking layer 132.

[0067] The insertion of the InAlAs lay r 131 between

the mesa stripe 151 and the InP(Fe) first current blocking layer 132 prevents the direct contact between the p-InP(Zn) second cladding layer 116, which is on top of the active region 114, and the first semi-insulating current bl cking layer InP(Fe) 132. This way, the Fe-Zn lateral interdiffusion that typically occurs in optoelectronic devices is suppressed since there is no contact between the two doped regions of the device.

[0068] At this point in the fabrication process, the subsequent steps proceed according to those described in the first embodiment and with respect to Figures 12-13. As such, once the InP(Si) second current blocking layer 134 (Figure 16) is grown and the mask 200 removed, a p-InP cladding layer 142 (Figure 17) is epitaxially grown on top of the second current blocking layer 134 and on top of the Q layer 118. Similarly, a p-InGaAsP or a p-InGaAs ohmic contact layer 144 is further grown over the p-InP cladding layer 142. Finally, an n-type electrode 162 and a p-type electrode 164 (Figure 17) are formed on the lower surface of the substrate 110 and on the upper surface of the ohmic contact layer 144, respectively, so to form a complete buried semi-insulating ridge heterostructure 202 (Figure 17).

[0069] Although the second embodiment has been described with reference to the mesa stripe 151 (Figures 14-17), which did not comprise an InAlAs layer (such as, for example, the InAlAs layer 115 of Figures 9-13 situated on top of the active region 114) or an InGaAlAs layer, it must be understood that the mesa stripe of the optoelectronic device may also comprise such an additional InAlAs or InGaAlAs layer situated on top of the active region. Such an example is illustrated in Figure 18, in which the active region 114 is bounded by two InAlAs layers 131, 115. This way, Fe-Zn lateral interdiffusion, as well as Zn diffusion into the active region, are minimized and the characteristics of the optoelectronic device are maximized.

[0070] In a third embodiment of the present invention, a plurality of InAlAs layers are grown around the mesa structure and in between different blocking layers forming the second crystal growth, optionally with a layer of InAlAs grown over the active region of the mesa structure. This embodiment is illustrated in Figure 19. A buried heterostructure laser diode 203 fabricated according to the third embodiment of the present invention comprises at least three InAlAs layers 115, 131, and 133. The formation of the InAlAs layers 115, 131 has been discussed before with respect to the first and second embodiments of the present invention (Figures 8-13; Figures 14-18) and it will not be described again. The current embodiment is characterized by the InAlAs layer 133, which is selectively grown on top of the semi-insulating InP(Fe) first current blocking layer 132 (Figure 19) and in lieu of the conventional n-InP(Si) second current blocking layer 134 (Figures 17-18). The ins rtion of an additional InAlAs layer as a current blocking layer further minimiz s the lateral Fe-Zn interdiffusi n and reduces any leakage current present in th device.

[0071] Figures 20-21 illustrate a fourth embodiment of the present invention, in which the Zn-Fe interdiffusion between the InP(Fe) first current blocking lay r 132 (Figure. 19) and the p-InP(Zn) cladding layer 142 (Figure 19) is completely eliminated. In this embodiment and as shown in Figure 20, after the epitaxial growth of the InAlAs layer 131, a selectively grown layer 136 of InP (Fe) first current blocking layer is formed over the InAlAs layer 131. This InP(Fe) first current blocking layer 136 is grown so that its contact with the mask 200 is minimal, for example, as illustrated in Figure 20, just a point C on each side of the mesa stripe. Of course, point C is part of a contact line (not shown) formed by the InP(Fe) first current blocking layer 136 and the mask 200. Next, the InAlAs layer 133 (Figure 20) that replaces the conventional n-InP(Si) second current layer 134 (Figures 17-18) is grown.

[0072] After removal of mask 200, the subsequent steps proceed according to those described in the first embodiment and with respect to Figure 13. As such, a p-InP(Zn) cladding layer 142 and a p-InGaAsP or a p-InGaAs ohmic contact layer 144 are further grown. B - cause of the selective growth of the InP(Fe) first current blocking layer 136, the contact regions D (Figure 5) situated on lateral sides of the mesa stripe are completely eliminated. Accordingly, the interdiffusion of the Fe and Zn atoms between the InP(Fe) first current blocking layer 136 and the p-InP(Zn) cladding layer 142 is eliminated. Further, the insertion of three InAlAs layers 115, 131, 133, of which two are on each side of the mesa stripe 151, suppresses any Fe-Zn interdiffusion that may be existent in the device, to ensure proper functionality.

[0073] The structure of Figure 21 is further completed with an n-type electrode 162 and a p-type electrode 164 (Figure 21) formed on the lower surface of the substrate 110 and on the upper surface of the ohmic contact layer 144, to form a buried semi-insulating ridge heterostructure 204, as illustrated in Figure 21.

[0074] Figures 22-23 illustrate yet a fifth embodiment of the present invention. In this embodiment, the additional InAlAs 133 layer is selectively grown after both the InP(Fe) first current blocking layer 132 and the n-InP(Si) second current blocking layer 134, but still as part of the second crystal growth. Thus, the InAlAs layer 133 (Figure 22) is grown before mask 200 is removed. After removal of the mask 200 (Figure 23), the p-InP(Zn) cladding layer 142 and the ohmic contact layer 144 are grown, followed by the formation of the n-type electrod 162 and the p-type electrode 164, to complete a buried semi-insulating ridge heterostructure 205 (Figure 23).

[0075] In a sixth embodiment of the present invention, which is illustrated in Figure 24, the additional InAlAs layer 133 is grown as part of the third crystal growth, and not as part of the second crystal growth as in th fifth embodiment. That is, in buried semi-insulating ridg heterostructure 206 of Figure 24, the InAlAs lay r 133 is grown after the removal f the mask 200 and befor the growth of the p-InP(Zn) cladding layer 142. As illus-

trated in Figure 24, th InAlAs layer 133 is grown over the mesa stripe 151 and the Q layer 118. Both InAlAs layers 115 and 131 suppress the diffusion of the Zn atoms from the p-InP(Zn) second cladding layer 116 into the active region 114, as well as the lateral diffusion of Zn from the mesa stripe and into the InP(Fe) first current blocking layer 132. Similarly, the InAlAs layer 133 further suppresses the interdiffusion of Zn and Fe atoms in the current blocking layers, that is between the InP(Fe) first current blocking layer 132 and the p-InP(Zn) cladding layer 142 of the buried semi-insulating ridge heterostructure 206.

[0076] So far the present invention has been described in the context of a buried semi-insulating ridge heterostructure, such as, for example, the buried semi-insulating ridge heterostructure 204 of Figure 21. However, the invention has broader applicability and can be used, for example, for the fabrication of a ridge structure for optoelectronic devices, such as electroabsorption modulators and detectors. In such case, which is illustrated in Figure 25, a ridge structure 209, which resides on an upper surface of an n-InP substrate 110, comprises a vertical mesa stripe 210 surrounded by insulating layers 211. The vertical mesa stripe 210 further comprises portions of a first cladding layer 112, of an active layer 114, of an InAlAs or InGaAlAs layer 115, of a second cladding layer 116 of p-InP(Zn), of a p-InP cladding layer 142, and of a p-InGaAsP or a p-InGaAs ohmic contact layer 144. Preferably, all of the above-mentioned layers are grown selectively by Metal Organic Vapor Phase Epitaxy (MOVPE). However, Liquid Phase Epitaxy (LPE), Vapor Phase Epitaxy (VPE), or Molecular Beam Epitaxy (MBE) could also be used as an alternative. The insulating layers 211 are formed preferably of polyimide by a deposition method.

[0077] The present invention provides a method for reducing the diffusion of Zn and the Zn-Fe interdiffusion among doped regions of laser devices, optical amplifiers, modulators, or detectors. The direct contact between Zn-doped layers and Fe-doped layers is prevented and the dopant atoms interdiffusion is suppressed.

[0078] Although the invention has been illustrated for an optoelectronic device fabricated on an n-type substrate, the invention could also be fabricated on a p-type or a semi-insulating type substrate, as well-known in the art. This, of course, will change the doping or conductivity of the operative layers in the fabricated device. Also, although the invention has been explained in the exemplary embodiments with reference to an InAlAs dopant blocking layer, the invention has equal applicability to optoelectronic devices using an InGaAlAs dopant blocking layer, or a combination of both InAlAs and InGaAlAs layers, as noted above.

[0079] The above description illustrates preferred embodiments which achi ve th features and advantages of the present invention. It is not intended that th present inv ntion be limited to the illustrated emb diments. Modifications and substitutions to specific process conditions and structures can be made without departing from the spirit and scope of the present invention.

[0080] For example, although all embodiments of the present invention include the InAlAs ar InGaAlAs layer 115 (Figures 9-13; Figures 18-25) situated on top of the active region of the optoelectronic device, it must be understood that the existence of such layer is optional in embodiments second through six, depending on the device characteristics and requirements. Similarly, as explained above, the embodiments of the present invention may include any number of additional InAlAs and/or InGaAlAs layers among the cladding and blocking layers that are doped with impurity atoms For example, an InAlAs and/or InGaAlAs layer may be formed between the cladding layer and the ohmic contact layer of the third crystal growth. Accordingly, the invention is not to be considered as being limited by the foregoing description and drawings, but is only limited by the scope of the appended claims.

Claims

1. An optoelectronic device comprising:

   a substrate of a first type conductivity; and
   a mesa structure provided on said substrate, said mesa structure having a least two sides and including an active region, said active region further being bounded on at least one side by a dopant blocking layer, said dopant blocking layer comprising a material selected from the group consisting of InAlAs and InGaAlAs.

2. The optoelectronic device of claim 1 further comprising a first current blocking layer at two sides of said mesa structure, a second current blocking layer of a first type conductivity formed over said first current blocking layer, and a cladding layer of a second type conductivity formed over said mesa structure and said second blocking layer.

3. The optoelectronic device of claim 1 further comprising a plurality of current blocking layers formed over said second current blocking layer.

4. The optoelectronic device of claim 1, wherein said dopant blocking layer is situated on top of said active region.

5. The optoelectronic device of claim 1 further comprising a doped second cladding layer of a second type conductivity in contact with said dopant blocking layer.

6. The optoelectronic device of claim 1, wherein said dopant blocking layer is situated between each of

said two sides of said mesa structure and said first current blocking layer.

7. The optoelectronic device of claim 1, wherein said doped second cladding layer is doped with a p-type dopant.

8. The optoelectronic device of claim 1, wherein said dopant blocking layer is an epitaxially grown layer.

9. The optoelectronic device of claim 1, wherein said dopant blocking layer has a thickness in the range of about 300 to 800 Angstroms.

10. The optoelectronic device of claim 1, wherein said active region includes a layer capable of emitting light.

11. The optoelectronic device of claim 1, wherein said active region includes a layer capable of absorbing light.

12. The optoelectronic device of claim 1, wherein said active region includes a layer capable of modulating light.

13. The optoelectronic device of claim 1, wherein said active region includes a layer capable of amplifying light.

14. The optoelectronic device of claim 1, wherein said dopant blocking layer comprises at least one InAlAs layer.

15. The optoelectronic device of claim 1, wherein said dopant blocking layer comprises at least one InGaAlAs layer.

16. The optoelectronic device of claim 1, wherein said dopant blocking layer comprises at least one layer of InAlAs and at least one layer of InGaAlAs.

17. A semiconductor optical device comprising:

a substrate of a first type conductivity; and
a mesa structure provided on said substrate, said mesa structure having at least two sides and including a dopant blocking layer, said dopant blocking layer comprising a material selected from the group consisting of InAlAs and InGaAlAs, said dopant blocking layer being further formed between an active region and a doped second cladding layer of a second type conductivity.

18. The semiconductor optical device of claim 17 further comprising a first current blocking layer at two sides of said mesa structure, a second current blocking layer of a first type conductivity formed over said first current blocking layer, and a cladding layer of a second type conductivity over said mesa structure and said second blocking layer.

19. The semiconductor optical device of claim 18 further comprising a plurality of current blocking layers formed over said second current blocking layer.

20. The semiconductor optical device of claim 17, wherein said doped second cladding layer is doped with a dopant selected from the group consisting of zinc, beryllium and magnesium.

21. The semiconductor optical device of claim 17, wherein said dopant blocking layer is an epitaxially grown layer.

22. The semiconductor optical device of claim 17, wherein said dopant blocking layer has a thickness in the range of about 300 to 800 Angstroms.

23. The semiconductor optical device of claim 17, wherein said active region includes a layer capable of emitting light.

24. The semiconductor optical device of claim 17, wherein said active region includes a layer capable of absorbing light.

25. The semiconductor optical device of claim 17, wherein said active region includes a layer capable of modulating light.

26. The semiconductor optical device of claim 17, wherein said active region includes a layer capable of amplifying light.

27. , The semiconductor optical device of claim 17, wherein said dopant blocking layer comprises at least one InAlAs layer.

28. The semiconductor optical device of claim 17, wherein said dopant blocking layer comprises at least one InGaAlAs layer.

29. The semiconductor optical device of claim 17, wherein said dopant blocking layer comprises at least one layer of InAlAs and at least one layer of InGaAlAs.

30. A method for forming a semiconductor laser comprising the steps of

forming a plurality of stacked layers over a substrate of a first type conductivity, at least one of said layers being an active region and at least another one of said layers being a dopant

blocking layer, said dopant blocking lay r comprising a material selected from the group consisting of InAlAs and InGaAlAs; and
etching said plurality of stacked layers and said substrate to form a mesa structure on said substrate.

31. The method of claim 30 further comprising the steps of forming a first current blocking layer at two sides of said mesa structure, forming a second current blocking layer of a first type conductivity over said first current blocking layer, and forming a cladding layer of a second type conductivity over said mesa and said second current blocking layer.

32. The method of claim 30, wherein said first type conductivity is n-type and said second type conductivity is p-type.

33. The method of claim 30, wherein said first type conductivity is p-type and said second type conductivity is n-type.

34. The method of claim 30 further comprising the step of forming a plurality of current blocking layers at said two sides of said mesa structure.

35. The method of claim 30, wherein said dopant blocking layer suppresses the diffusion of dopants from a second cladding layer into said active region, said second cladding layer being formed on top of and in contact with said dopant blocking layer.

36. The method of claim 35, wherein said second cladding layer is grown selectively by metal organic vapor phase epitaxy.

37. The method of claim 35, wherein said second cladding layer is of a second type conductivity.

38. The method of claim 35 further comprising the step of doping said second cladding layer.

39. The method of claim 30, wherein said dopant blocking layer is epitaxially grown.

40. The method of claim 30, wherein said dopant blocking layer is grown selectively by metal organic vapor phase epitaxy.

41. The method of claim 30, wherein said dopant blocking layer is grown to a thickness in the range of about 300 to 800 Angstroms.

42. Th method of claim 30, wherein said active region includes a layer capable of emitting light wh n excited.

43. Th method of claim 30, wherein said activ r gion includes a layer capable of absorbing light.

44. The method of claim 30, wherein said active region includes a layer capable of modulating light.

45. The method of claim 30, wherein said active region includes a layer capable of amplifying light.

46. The method of claim 30, wherein said dopant blocking layer comprises at least one InAlAs layer.

47. The method of claim 30, wherein said dopant blocking layer comprises at least one InGaAlAs layer,

48. The method of claim 30, wherein said dopant blocking layer comprises at least one layer of InAlAs and at least one layer of InGaAlAs.

49. A semiconductor optical device comprising:

a substrate of a first type conductivity;
a mesa structure provided on said substrate, said mesa structure having two sides and including an active region; and
a first dopant blocking layer at two sides of said mesa structure, said dopant blocking lay r comprising a material selected from the group consisting of InAlAs and InGaAlAs.

50. The semiconductor optical device of claim 49 further comprising a plurality of current blocking layers formed over said second current blocking layer.

51. The semiconductor optical device of claim 49, wherein said first dopant blocking layer comprises at least one InAlAs layer.

52. The semiconductor optical device of claim 49, wherein said first dopant blocking layer comprises at least one InGaAlAs layer.

53. The semiconductor optical device of claim 49, wherein said first dopant blocking layer is an epitaxially grown layer.

54. The semiconductor optical device of claim 49, wherein said first dopant blocking layer has a thickness in the range of about 300 to 3000 Angstroms.

55. The semiconductor optical device of claim 49 further comprising a first current blocking layer formed over said first dopant blocking layer, a second current blocking layer of a first type conductivity formed over said first curr nt blocking layer, and a cladding layer of a sec nd type conductivity formed over said mesa structure and said second blocking layer.

56. The semiconductor optical device of claim 55, wherein said first current blocking layer is doped.

57. The semiconductor optical device of claim 56, wherein said dopant is a semi-insulating type dopant.

58. The semiconductor optical device of claim 57, wherein said first current blocking layer is an InP (Fe) layer.

59. The semiconductor optical device of claim 55, wherein said second current blocking layer is doped with a dopant selected from the group consisting of silicon, sulfur and tin.

60. The semiconductor optical device of claim 55, wherein said mesa structure further comprises a second cladding layer formed over said active region.

61. The semiconductor optical device of claim 55, wherein said mesa structure further comprises a second dopant blocking layer formed in between said second cladding layer and said active region.

62. The semiconductor optical device of claim 61, wherein said second dopant blocking layer comprises a material selected from the group consisting of InAlAs and InGaAlAs.

63. The semiconductor optical device of claim 61, wherein said second dopant blocking layer comprises at least one InAlAs layer.

64. The semiconductor optical device of claim 61, wherein said second dopant blocking layer comprises at least one InGaAlAs layer.

65. The semiconductor optical device of claim 61, wherein said second dopant blocking layer comprises at least one layer of InAlAs and at least one layer of InGaAlAs.

66. The semiconductor optical device of claim 49, wherein said active region includes a layer capable of emitting light.

67. The semiconductor optical device of claim 49, wherein said active region includes a layer capable of absorbing light.

68. The semiconductor optical device of claim 49, wherein said active region includes a layer capable of m dulating light.

69. The s miconductor optical device of claim 49, wherein said active region includes a layer capable of amplifying light.

70. A semiconductor optical devic comprising:

a substrate of a first type conductivity;
a mesa structure provided on said substrate, said mesa structure having two sides and including an active region, said mesa structure further including a first dopant blocking layer in contact with said active region, said first dopant blocking layer comprising a material selected from the group consisting of InAlAs and InGaAlAs; and
a second dopant blocking layer at two sides of said mesa structure.

71. The semiconductor optical device of claim 70 further comprising a first current blocking layer formed over said second dopant blocking layer, a third dopant blocking layer formed over said first current blocking layer, and a cladding layer of a second type conductivity formed over said mesa structure and said third dopant blocking layer.

72. The semiconductor optical device of claim 71 further comprising a plurality of current blocking layers formed in between said first current blocking layer and said third dopant blocking layer.

73. The semiconductor optical device of claim 71, wherein said second dopant blocking layer comprises a material selected from the group consisting of InAlAs and InGaAlAs.

74. The semiconductor optical device of claim 71, wherein said third dopant blocking layer comprises a material selected from the group consisting of InAlAs and InGaAlAs.

75. The semiconductor optical device of claim 71, wherein said first dopant blocking layer is situated on top of said active region.

76. The semiconductor optical device of claim 71 further comprising a doped second cladding layer of a second type conductivity in contact with said first and second dopant blocking layers.

77. The semiconductor optical device of claim 76, wherein said doped second cladding layer is doped with a p-type dopant.

78. The semiconductor optical device of claim 71, wherein said second dopant blocking layer has a thickn ss in the rang of ab ut 300 to 3000 Angstroms.

79. The semiconductor optical device of claim 71,

wherein said third dopant blocking layer has a thickness in the range of about 300 to 3000 Angstroms.

80. The semiconductor optical device of claim 70, wherein said first dopant blocking layer has a thickness in the range of about 300 to 800 Angstroms.

81. The semiconductor optical device of claim 70, wherein said active region includes a layer capable of emitting light when excited.

82. The semiconductor optical device of claim 70, wherein said active region includes a layer capable of absorbing light.

83. The semiconductor optical device of claim 70, wherein said active region includes a layer capable of modulating light.

84. The semiconductor optical device of claim 70, wherein said active region includes a layer capable of amplifying light.

85. A semiconductor optical device comprising:

a substrate of a first type conductivity;
a mesa structure provided on said substrate, said mesa structure having two sides and including an active region;
a first current blocking layer at two sides of said mesa structure;
a second current blocking layer of a first type conductivity formed over said first current blocking layer,
a first dopant blocking layer formed over said second current blocking layer, said first dopant blocking layer comprising a material selected from the group consisting of InAlAs and InGaAlAs; and
a cladding layer of a second type conductivity formed over said mesa structure and said first dopant blocking layer.

86. The semiconductor optical device of claim 85 further comprising a second dopant blocking layer on top of said active region.

87. The semiconductor optical device of claim 86, wherein said second dopant blocking layer comprises a material selected from the group consisting of InAlAs and InGaAlAs.

88. The semiconductor optical device of claim 86, wherein said second dopant blocking layer has a thickness in the range of about 300 to 800 Angstroms.

89. The semiconductor optical device of claim 85 further comprising a third dopant blocking layer between said two sides of said mesa stripe and said first current blocking layer.

90. The semiconductor optical device of claim 89, wherein said third dopant blocking layer comprises a material selected from the group consisting of InAlAs and InGaAlAs.

91. The semiconductor optical device of claim 89, wherein said third dopant blocking layer has a thickness in the range of about 300 to 3000 Angstroms.

92. The semiconductor optical device of claim 86 further comprising a doped first cladding layer of a second type conductivity in contact with said second dopant blocking layer.

93. The semiconductor optical device of claim 92, wherein said doped second cladding layer is doped with a p-type dopant.

94. The semiconductor optical device of claim 85, wherein said first dopant blocking layer has a thickness in the range of about 300 to 3000 Angstroms.

95. An optoelectronic device comprising:

a substrate of a first type conductivity,
a mesa structure provided on said substrate, said mesa structure having two sides and including an active region, said active region further being bounded on at least one side by a dopant blocking layer, said dopant blocking layer comprising a material selected from the group consisting of InAlAs and InGaAlAs; and
an insulating layer at two sides of said mesa structure.

96. The optoelectronic device of claim 95, wherein said mesa structure further includes a cladding layer of a second type conductivity formed over said mesa structure, and an ohmic contact layer formed over said cladding layer.

97. The optoelectronic device of claim 95, wherein said dopant blocking layer is situated on top of said active region.

98. The optoelectronic device of claim 95 further comprising a doped second cladding layer of a second type conductivity in contact with said dopant blocking layer.

99. The optoelectronic device of claim 98, wherein said doped second cladding layer is doped with a p-type dopant.

100. The optoelectronic device of claim 95, wherein said dopant blocking layer is an epitaxially grown layer.

101. The optoelectronic device of claim 95, wherein said dopant blocking layer has a thickness in the range of about 300 to 800 Angstroms.

102. The optoelectronic device of claim 95, wherein said active region includes a layer capable of absorbing light.

103. The optoelectronic device of claim 95, wherein said active region includes a layer capable of modulating light.

104. The optoelectronic device of claim 95, wherein said insulating layer is formed of polyimide.

FIG. 1

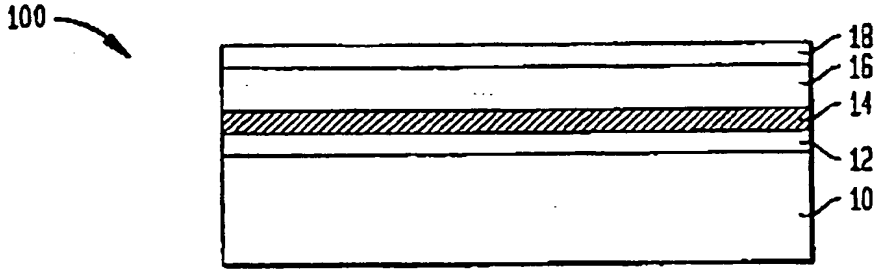


FIG. 2

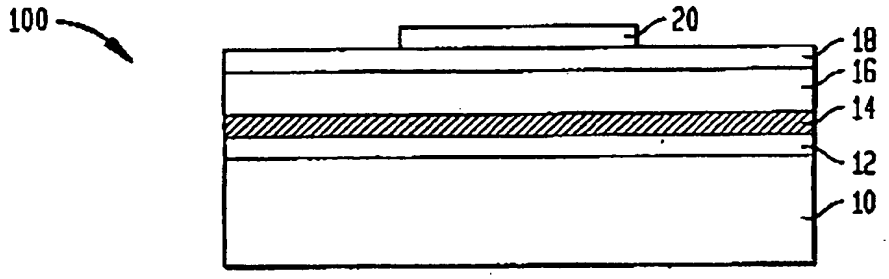


FIG. 3

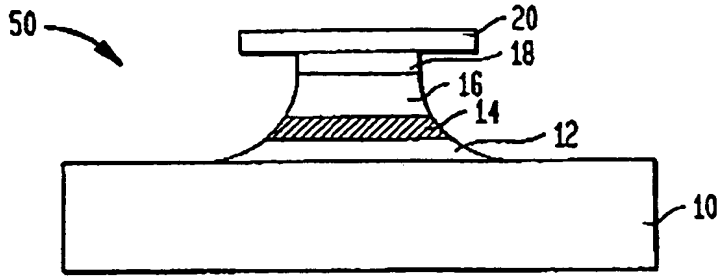


FIG. 4

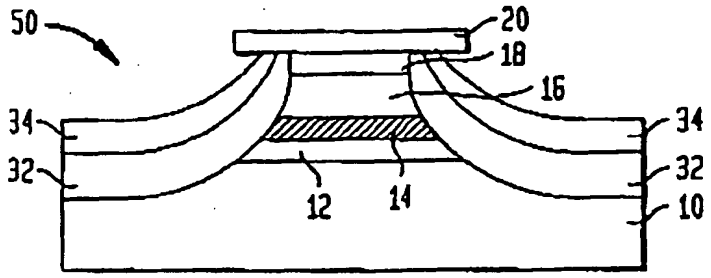


FIG. 5

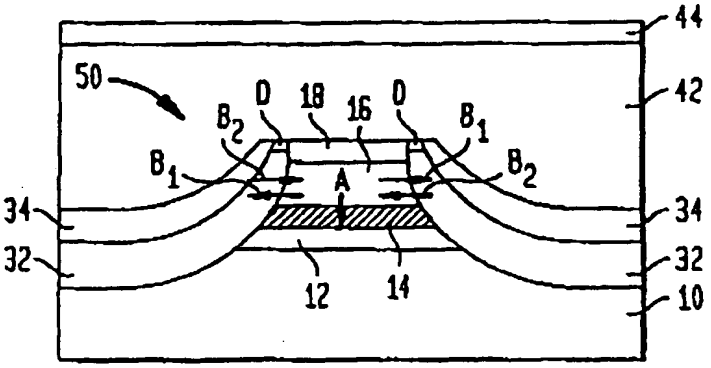


FIG. 6
(PRIOR ART)

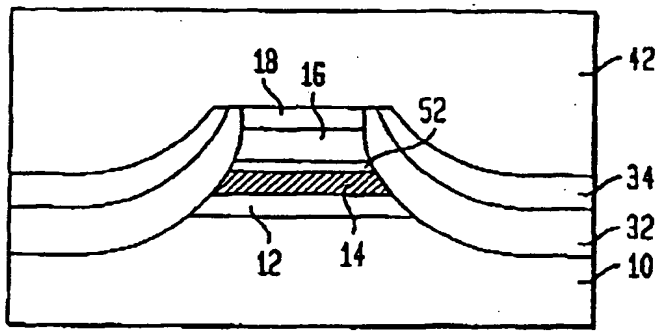


FIG. 7
(PRIOR ART)

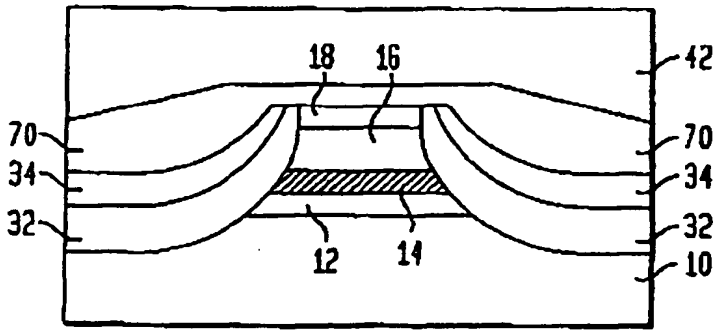


FIG. 8

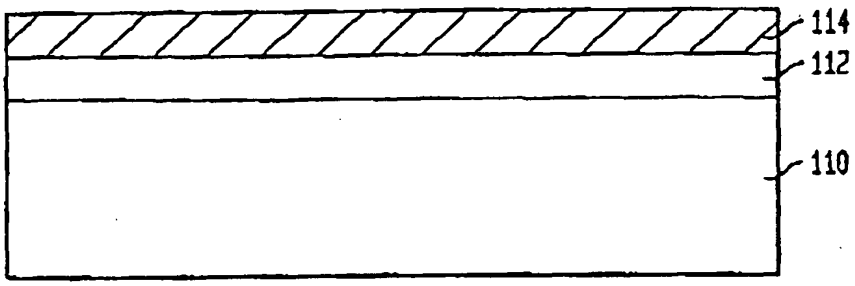


FIG. 9

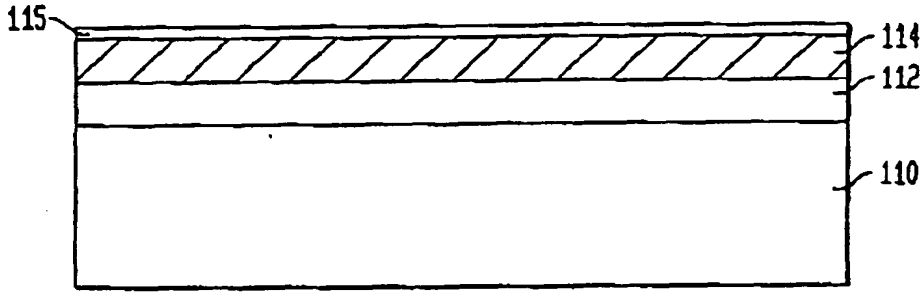


FIG. 10

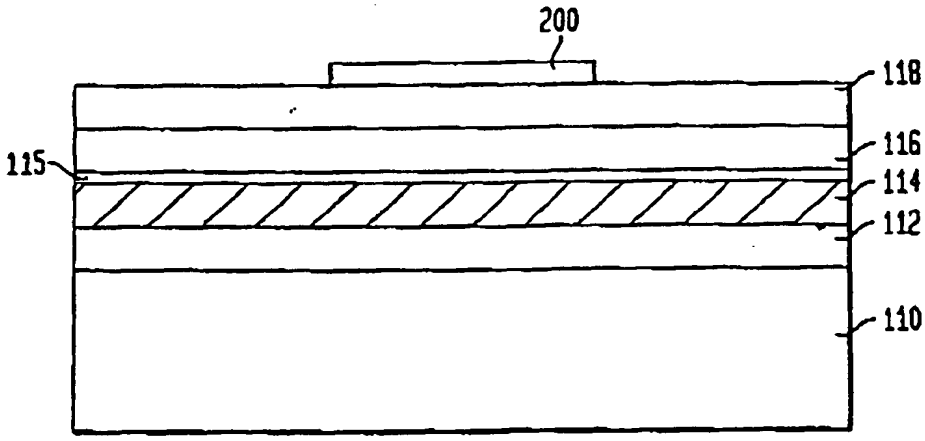


FIG. 11

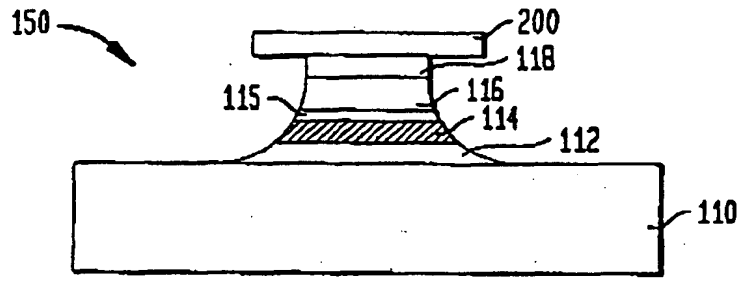


FIG. 12

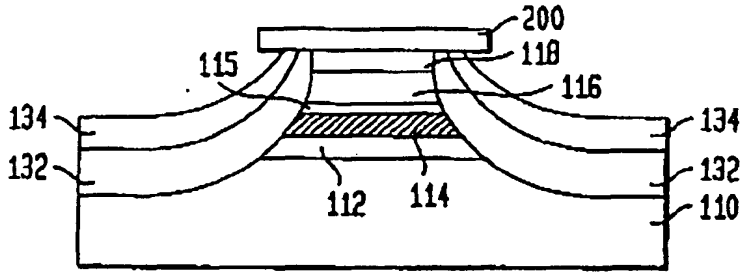


FIG. 13

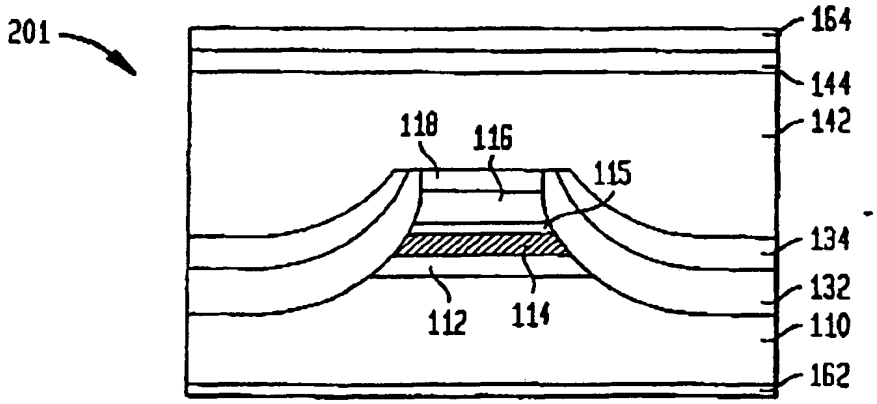


FIG. 14

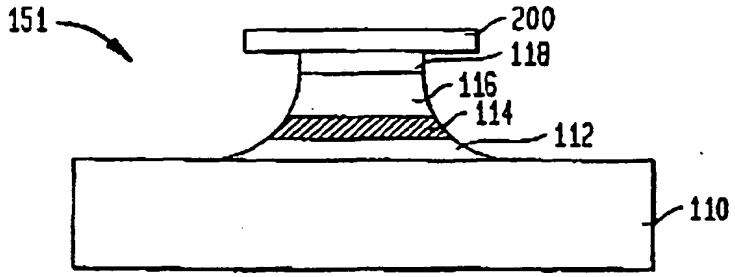


FIG. 15

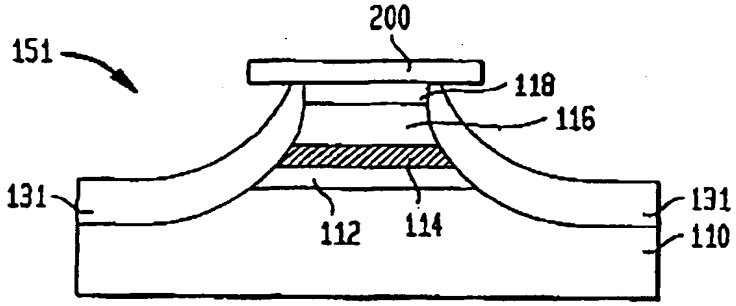


FIG. 16

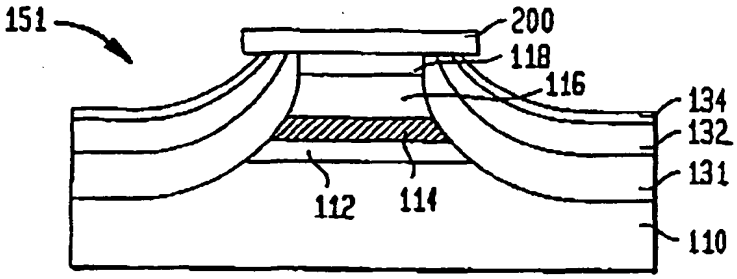


FIG. 17

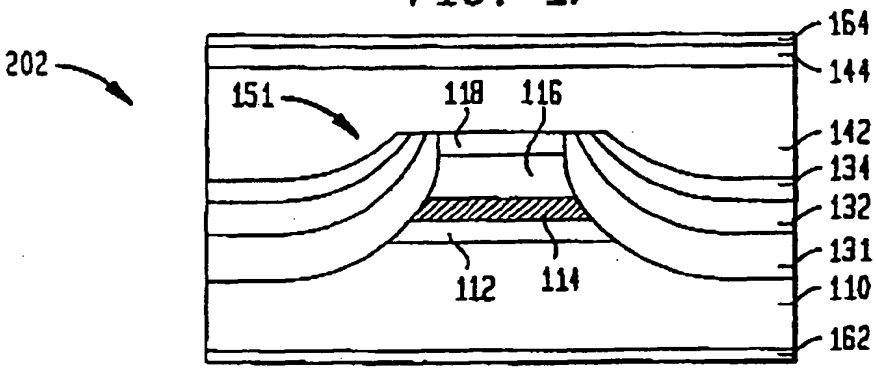


FIG. 18

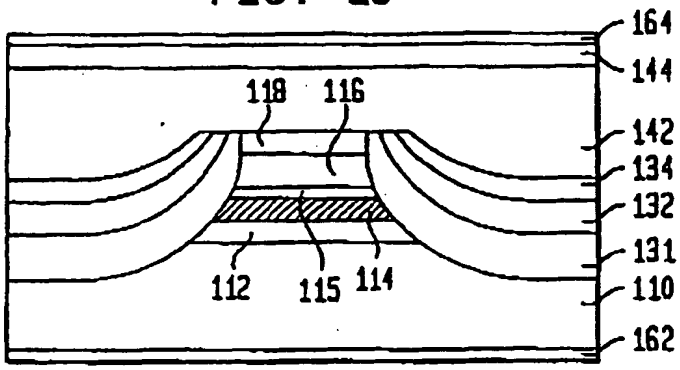


FIG. 19

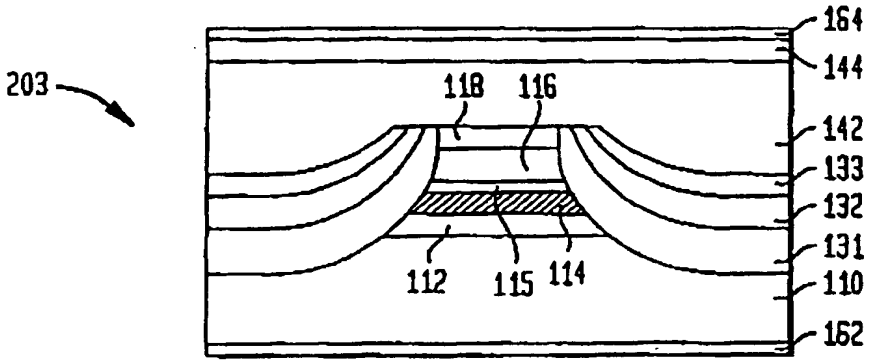


FIG. 20

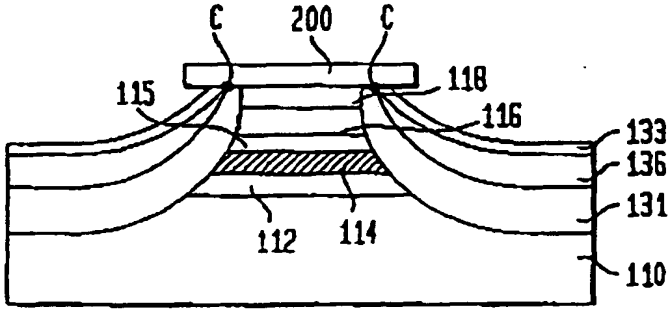


FIG. 21

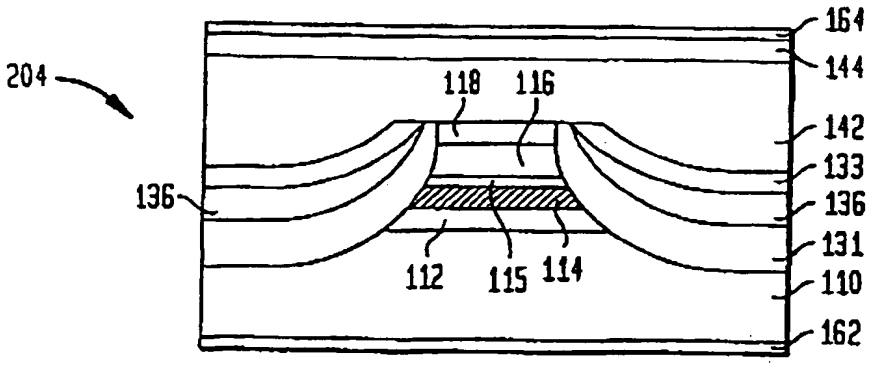


FIG. 22

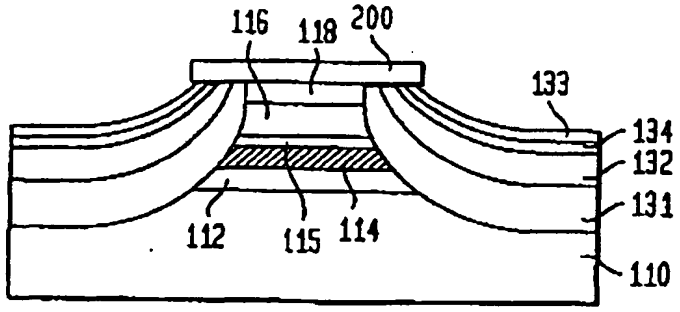


FIG. 23

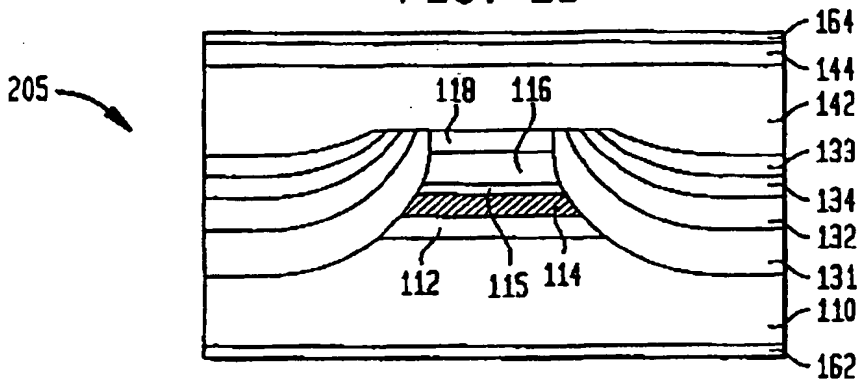


FIG. 24

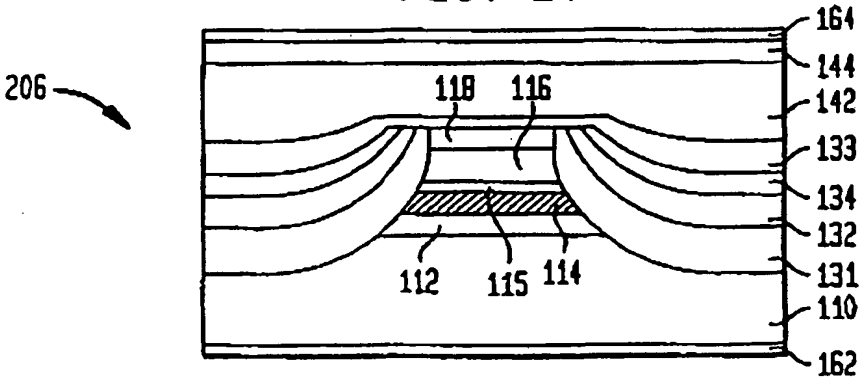
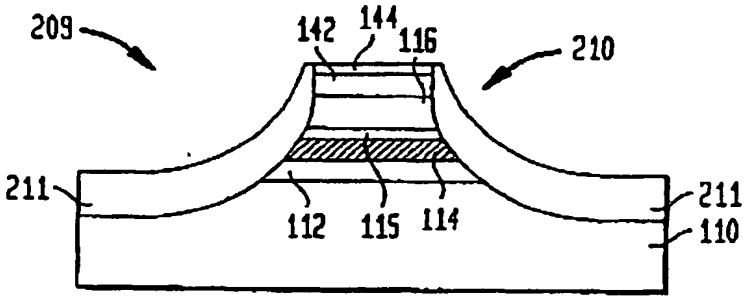


FIG. 25



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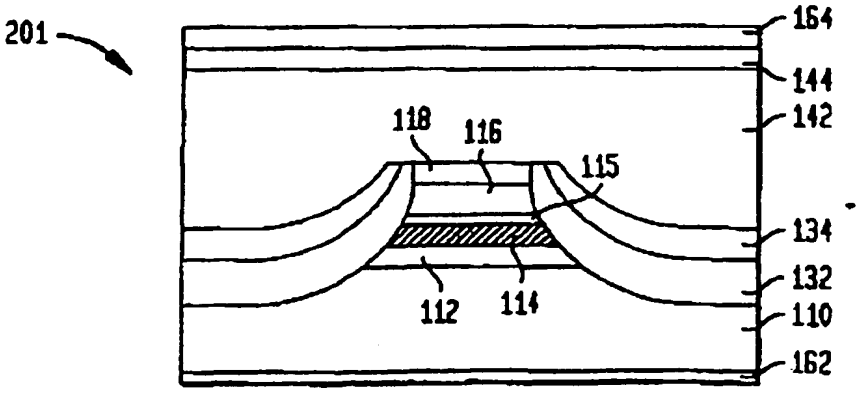
(54) **Dopant diffusion blocking for optoelectronic devices using InAlAs or InGaAlAs**

(57) A method for decreasing the diffusion of dopant atoms in the active region, as well as the interdiffusion of different types of dopant atoms among adjacent doped regions, of optoelectronic devices is disclosed. The method of the present invention employs a plurality of InAlAs and/or InGaAlAs layers to avoid the direct contact between the dopant atoms and the active region, and between the dopant atoms in adjacent blocking structures of optoelectronic devices. A semi-insulating buried ridge structure, as well as a ridge structure, in which the interdiffusion of different types of dopant atoms is suppressed are also disclosed.

FIG. 13



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EUROPEAN SEARCH REPORT

Application Number
EP 01 30 3131

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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	23 November 2001	Hervé, D

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